AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended): An apparatus in a microprocessor for executing programmed native instructions that are provided directly to the microprocessor via an external instruction bus, the apparatus comprising:

instruction translation logic, configured to retrieve macro instructions provided via the external instruction bus, and configured to decode each of said macro instructions into associated native instructions for execution by the microprocessor, wherein said instruction translation logic decodes a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the programmed native instructions, and wherein said memory address is explicitly prescribed by contents of an architectural register, said contents and said architectural register being prescribed by a macro instruction; and

bypass logic, coupled to said instruction translation logic, configured to disable said instruction translation logic upon detection of said native bypass macro instruction, and configured to provide the programmed native instructions for execution by the microprocessor, thereby bypassing said instruction translation logic.

2. (original): The apparatus as recited in claim 1, wherein the programmed native instructions are provided from a memory to the external instruction bus.

3. (previously presented): The apparatus as recited in claim 1, wherein execution of said native bypass macro instruction causes the microprocessor to transfer program control to the programmed native instructions.

4. (previously presented): The apparatus as recited in claim 3, wherein said bypass logic comprises:

mode detection logic, configured to detect said native bypass macro instruction within a macro instruction sequence that is provided to said instruction translation logic, wherein, upon detection of said native bypass macro instruction, said mode detection logic directs said instruction translation logic to cease decoding said macro instruction sequence following decoding of said native bypass macro instruction.

5. (previously presented): The apparatus as recited in claim 4, wherein said unconditional jump native instruction directs the microprocessor to transfer program control to said memory address.

6. (currently amended): The apparatus as recited in claim 5, wherein the microprocessor comprises an x86-compatible microprocessor, and wherein said architectural register comprises register EAX~~where said memory address is provided in an architectural register~~.

7. (original): The apparatus as recited in claim 4, wherein said bypass logic further comprises:

a native instruction router, coupled to said mode detection logic, configured to receive the programmed native instructions, and configured to route the programmed native instructions to a native instruction bus.

8. (original): The apparatus as recited in claim 4, wherein, said mode detection logic is also configured to detect a native branch return macro instruction, said native branch return macro instruction following the programmed native instructions, wherein, upon detection of said native branch return macro instruction, said mode detection logic directs said instruction translation logic to resume decoding said macro instruction sequence.

9. (original): The apparatus as recited in claim 8, wherein said instruction translation logic decodes said native branch return macro instruction into a native branch return native instruction, and wherein said native branch return native instruction directs the microprocessor to transfer program control to a return address.

10. (original): The apparatus as recited in claim 9, wherein said return address designates a next macro instruction, said next macro instruction being within said macro instruction sequence and following said native branch macro instruction.

11. (currently amended): An apparatus, for allowing a micro instruction to be directly provided from an external instruction bus to execution logic within a pipeline microprocessor, the apparatus comprising:

a translator, for receiving macro instructions from a macro instruction bus, and for translating each of said macro instructions into associated micro instructions, said associated micro instructions being provided to the execution logic via a micro instruction bus, wherein said translator translates a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the micro instruction, and wherein said memory address is explicitly prescribed by contents of an architectural register, said contents and said architectural register being prescribed by a macro instruction; and

bypass logic, coupled to said translator, for routing the micro instruction to the execution logic, said bypass logic comprising:

a mode detector, for detecting said native bypass macro instruction, and for directing that said translator cease instruction translation; and

native instruction routing logic, coupled to said mode detector, for receiving said micro instruction from said macro instruction bus, and for providing said micro instruction to said micro instruction bus, thereby circumventing said translator.

12. (original): The apparatus as recited in claim 11, wherein the external instruction bus typically provides said macro instructions to the microprocessor.

13. (previously presented): The apparatus as recited in claim 11, wherein the execution logic executes said unconditional jump native instruction by transferring program control to said memory address that contains the micro instruction.

14. (currently amended): The apparatus as recited in claim 13, wherein the pipeline microprocessor comprises an x86-compatible microprocessor, and wherein said architectural register comprises register EAX~~said memory address is provided in an architectural register~~.

15. (original): The apparatus as recited in claim 11, wherein, said mode detector is configured to detect a native branch return macro instruction, wherein, upon detection of said native branch return macro instruction, said mode detection logic directs said translator to resume instruction translation.

16. (original): The apparatus as recited in claim 15, wherein the execution logic executes said native branch return macro instruction by transferring program control to a return memory address.

17. (original): The apparatus as recited in claim 16, wherein said return memory address contains a next macro instruction.

18. (currently amended): A microprocessor for executing micro instructions directly from memory, the microprocessor comprising:

translation logic, for receiving macro instructions from the memory, and for decoding said macro instructions into corresponding micro instructions for execution by the microprocessor;

mode detection logic, coupled to said translation logic, for detecting bypass macro instructions, and for directing the microprocessor to execute the micro instructions directly from the memory rather than via said translation logic, said bypass macro instructions comprising:

a native branch macro instruction, directing that program control be transferred to a target address, wherein said translation logic decodes said native branch macro instruction into an unconditional jump native instruction directing that program control be transferred to said target address, and wherein said target address contains the micro instructions, and wherein said target address is explicitly prescribed by contents of an architectural register, said contents and said architectural register being prescribed by a macro instruction; and

a native branch return macro instruction, directing that program control be transferred to a return address; and

an instruction router, coupled to said mode detection logic, for receiving the micro instructions, and for routing the micro instructions to execution logic, thereby bypassing said translation logic.

19. (original): The apparatus as recited in claim 18, wherein said mode detection logic, upon execution of said native branch macro instruction, directs said translation logic to cease decoding said macro instructions.

20. (cancelled)

21. (currently amended): The apparatus as recited in claim 18, wherein the microprocessor comprises an x86-compatible microprocessor, and wherein said architectural register comprises register EAX~~where said target address is provided in an architectural register~~.

22. (original): The apparatus as recited in claim 18, wherein said instruction router routes the micro instructions from a macro instruction bus to a micro instruction bus.

23. (original): The apparatus as recited in claim 18, wherein said mode detection logic, upon execution of said native branch return macro instruction, directs said translation logic to resume decoding said macro instructions.

24. (original): The apparatus as recited in claim 23, wherein said return address designates a next macro instruction, said next macro instruction being one of said macro instructions.